**Nome:** Matheus Soares Santos **TIA:** 31895263

**PIC18F4550 - Mnemônicos (opcodes)**

**OPCODE FIELD DESCRIPTIONS**

|  |  |
| --- | --- |
| **Field** | **Description** |
| a | RAM access bit  a = 0: RAM location in Access RAM (BSR register is ignored)  a = 1: RAM bank is specified by BSR register |
| bbb | Bit address within an 8-bit file register (0 to 7). |
| BSR | Bank Select Register. Used to select the current RAM bank. |
| C, DC, Z, OV, N | ALU Status bits: **C**arry, **D**igit **C**arry, **Z**ero, **O**verflow, **N**egative. |
| d | Destination select bit  d = 0: store result in WREG  d = 1: store result in file register f |
| dest | Destination: either the WREG register or the specified register file location. |
| f | 8-bit register file address (00h to FFh) or 2-bit FSR designator (0h to 3h). |
| fs | 12-bit register file address (000h to FFFh). This is the source address. |
| fd | 12-bit register file address (000h to FFFh). This is the destination address. |
| GIE | Global Interrupt Enable bit |
| k | Literal field, constant data or label (may be either an 8-bit, 12-bit or a 20-bit value). |
| label | Label name. |
| Mm  \*  \*+  \*-  +\* | The mode of the TBLPTR register for the table read and table write instructions.  Only used with table read and table write instructions:  No change to register (such as TBLPTR with table reads and writes)  Post-Increment register (such as TBLPTR with table reads and writes)  Post-Decrement register (such as TBLPTR with table reads and writes)  Pre-Increment register (such as TBLPTR with table reads and writes) |
| n | The relative address (2’s complement number) for relative branch instructions or the direct address for Call/Branch and Return instructions. |
| PC | Program Counter. |
| PCL | Program Counter Low Byte. |
| PCH | Program Counter High Byte. |
| PCLATH | Program Counter High Byte Latch. |
| PCLATU | Program Counter Upper Byte Latch. |
| PD | Power-Down bit. |
| PRODH | Product of Multiply High Byte. |
| PRODL | Product of Multiply Low Byte. |
| s | Fast Call/Return mode select bit  s = 0: do not update into/from shadow registers  s = 1: certain registers loaded into/from shadow registers (Fast mode) |
| TBLPTR | 21-bit Table Pointer (points to a program memory location). |
| TABLAT | 8-bit Table Latch. |
| TO | Time-out bit. |
| TOS | Top-of-Stack. |
| u | Unused or unchanged. |
| WDT | Watchdog Timer. |
| WREG | Working register (accumulator). |
| x | Don’t care (‘0’ or ‘1’). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools. |
| zs | 7-bit offset value for indirect addressing of register files (source). |
| zd | 7-bit offset value for indirect addressing of register files (destination). |
| ( ) | Optional argument. |
| [text] | Indicates an indexed address. |
| (text) | The contents of text. |
| [expr] <n> | Specifies bit n of the register indicated by the pointer expr. |
| → | Assigned to. |
| < > | Register bit field. |
| ∈ | In the set of. |
| italics | User-defined term (font is Courier). |

**GENERAL FORMAT FOR INSTRUCTIONS**

Byte-oriented file register operations

15 10 9 8 7 0

|  |  |  |  |
| --- | --- | --- | --- |
| OPCODE | d | a | f (FILE #) |

d = 0 for result destination to be WREG register

d = 1 for result destination to be file register (f)

a = 0 to force Access Bank

a = 1 for BSR to select bank

f= 8-bit file register address

Bit-oriented file register operations

15 12 11 9 8 7 0

|  |  |  |  |
| --- | --- | --- | --- |
| OPCODE | b (BIT #) | a | f (FILE #) |

b = 3-bit position of bit in file register (f)

a = 0 to force Access Bank

a = 1 for BSR to select bank

f= 8-bit file register address

Literal operations

15 8 7 0

|  |  |
| --- | --- |
| OPCODE | k (literal) |

k = 8-bit immediate value

**Control** operations

**CALL**, GOTO and **Branch** operations

15 8 7 0

|  |  |
| --- | --- |
| OPCODE | n<7:0> (literal) |

15 12 11 0

|  |  |
| --- | --- |
| 1111 | n<19:8> (literal) |

n = 20-bit immediate value

15 8 7 0

|  |  |  |
| --- | --- | --- |
| OPCODE | S | n<7:0> (literal) |

15 12 11 0

|  |  |
| --- | --- |
| 1111 | n<19:8> (literal) |

S = Fast bit

15 11 10 0

|  |  |
| --- | --- |
| OPCODE | n<10:0> (literal) |

15 8 7 0

|  |  |
| --- | --- |
| 1111 | n<19:8> (literal) |

**PIC18F4550 INSTRUCTION SET**

|  |  |
| --- | --- |
| **Mnemonic, Operands** | **Description** |

BYTE-ORIENTED OPERANDS

|  |  |
| --- | --- |
| ADDWF f,d,a  ADDWFC f,d,a  ANDWF f,d,a  CLRF f,a  COMF f,d,a  CPFSEQ f,a  CPFSGT f,a  CPFSLT f,a  DECF f,d,a  DECFSZ f,d,a  DCFSNZ f,d,a  INCF f,d,a  INCFSZ f,d,a  INFSNZ f,d,a  IORWF f,d,a  MOVF f,d,a  MOVFF fs, fd  MOVWF f,a  MULWF f,a  NEGF f,a  RLCF f,d,a  RLNCF f,d,a  RRCF f,d,a  RRNCF f,d,a  SETF f,a  SUBFWB f,d,a  SUBWF f,d,a  SUBWFB f,d,a  SWAPF f,d,a  TSTFSZ f,a  XORWF f,d,a  BCF f,b,a  BSF f,b,a  BTFSC f,b,a  BTFSS f,b,a  BTG f,d,a | Add WREG and f  Add WREG and Carry bit to f  AND WREG with f  Clear f  Complement f  Compare f with WREG, Skip =  Compare f with WREG, Skip >  Compare f with WREG, Skip <  Decrement f  Decrement f, Skip if 0  Decrement f, Skip if Not 0  Increment f  Increment f, Skip if 0  Increment f, Skip if Not 0  Inclusive OR WREG with f  Move f  Move fs (source) to 1st word  fd (destination) 2nd word  Move WREG to f  Multiply WREG with f  Negate f  Rotate Left f through Carry  Rotate Left f (No Carry)  Rotate Right f through Carry  Rotate Right f (No Carry)  Set f  Subtract f from WREG with Borrow  Subtract WREG from f  Subtract WREG from f with Borrow  Swap Nibbles in f  Test f, Skip if 0  Exclusive OR WREG with f  Bit Clear f  Bit Set f  Bit Test f, Skip if Clear  Bit Test f, Skip if Set  Bit Toggle f |

CONTROL OPERATIONS

|  |  |
| --- | --- |
| BC n  BN n  BNC n  BNN n  BNOV n  BNZ n  BOV n  BRA n  BZ n  CALL n, s  CLRWDT ---  DAW ---  GOTO n  NOP ---  NOP ---  POP ---  PUSH ---  RCALL n  RESET  RETFIE s  RETLW k  RETURN s  SLEEP --- | Branch if Carry  Branch if Negative  Branch if Not Carry  Branch if Not Negative  Branch if Not Overflow  Branch if Not Zero  Branch if Overflow  Branch Unconditionally  Branch if Zero  Call Subroutine 1st word  2nd word Clear  Watchdog Timer  Decimal Adjust WREG  Go to Address 1st word  2nd word  No Operation  No Operation  Pop Top of Return Stack (TOS)  Push Top of Return Stack (TOS)  Relative Call  Software Device Reset  Return from Interrupt Enable  Return with Literal in WREG  Return from Subroutine  Go into Standby mode |

LITERAL OPERATIONS

|  |  |
| --- | --- |
| ADDLW k  ANDLW k  IORLW k  LFSR f, k  MOVLB k  MOVLW k  MULLW k  RETLW k  SUBLW k  XORLW k | Add Literal and WREG  AND Literal with WREG  Inclusive OR Literal with WREG  Move Literal (12-bit) 2nd word to FSR(f) 1st word  Move Literal to BSR<3:0>  Move Literal to WREG  Multiply Literal with WREG  Return with Literal in WREG  Subtract WREG from Literal  Exclusive OR Literal with WREG |

DATA MEMORY ↔ PROGRAM MEMORY OPERATIONS

|  |  |
| --- | --- |
| TBLRD\*  TBLRD\*+  TBLRD\*-  TBLRD+\*  TBLWT\*  TBLWT\*+  TBLWT\*-  TBLWT+\* | Table Read  Table Read with Post-Increment  Table Read with Post-Decrement  Table Read with Pre-Increment  Table Write  Table Write with Post-Increment  Table Write with Post-Decrement  Table Write with Pre-Increment |